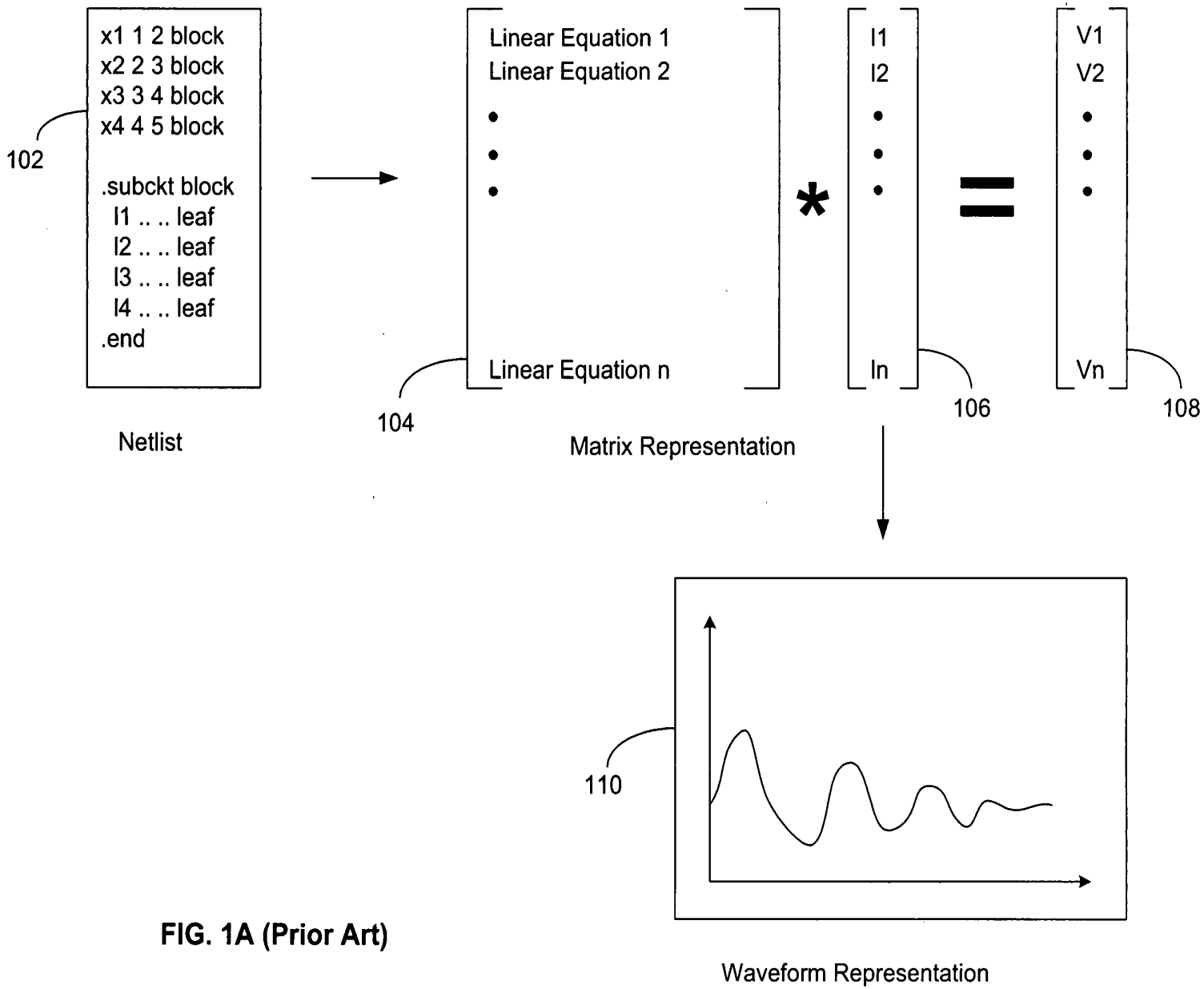


FIG. 1A (Prior Art)

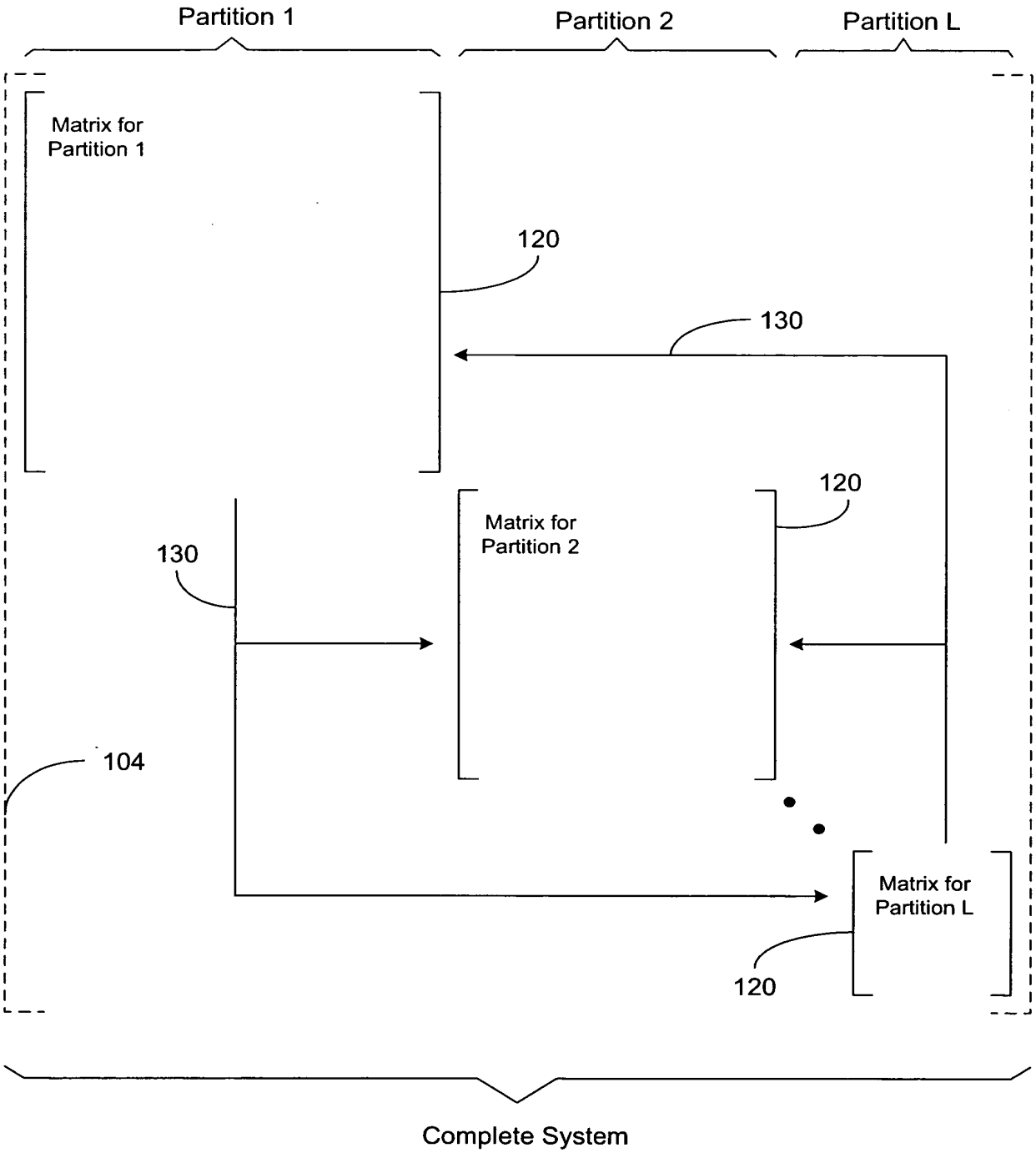


FIG. 1B (Prior Art)

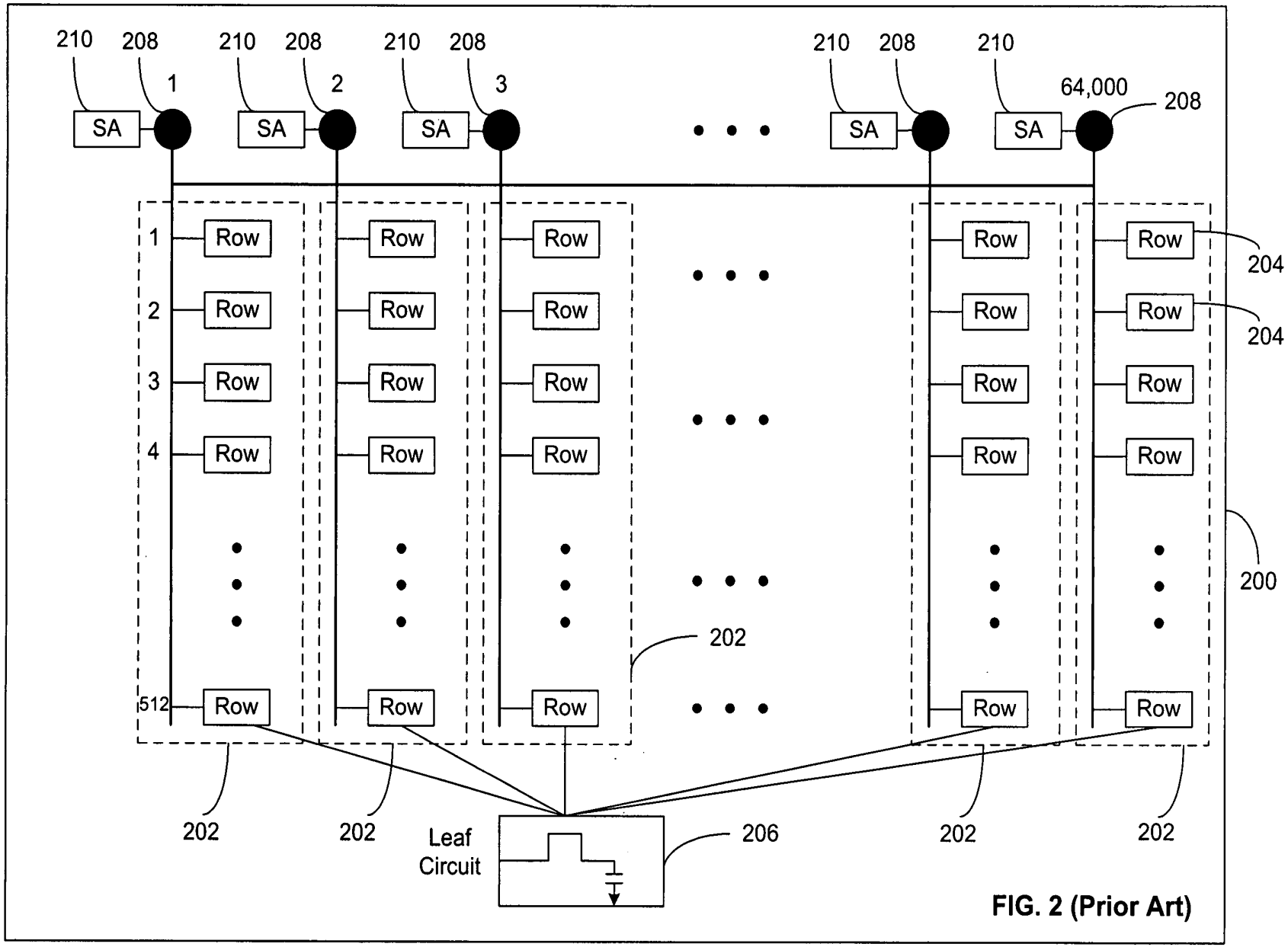
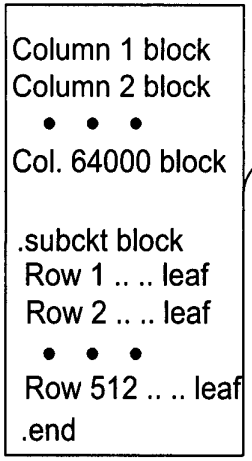


FIG. 2 (Prior Art)



Netlist Representation

FIG. 3A (Prior Art)

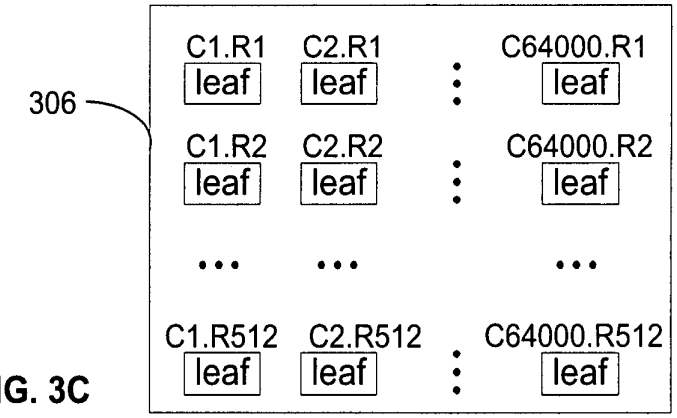


FIG. 3C (Prior Art)

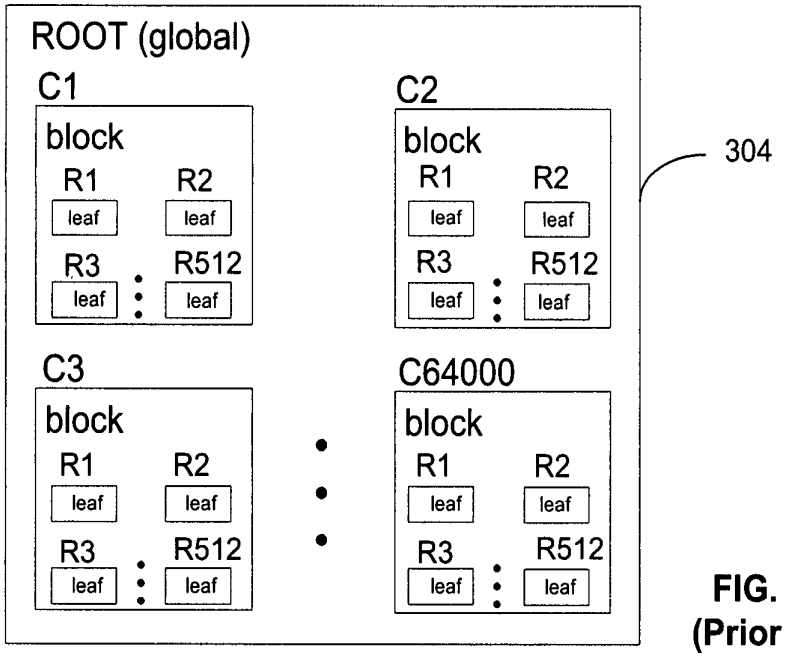


FIG. 3B (Prior Art)

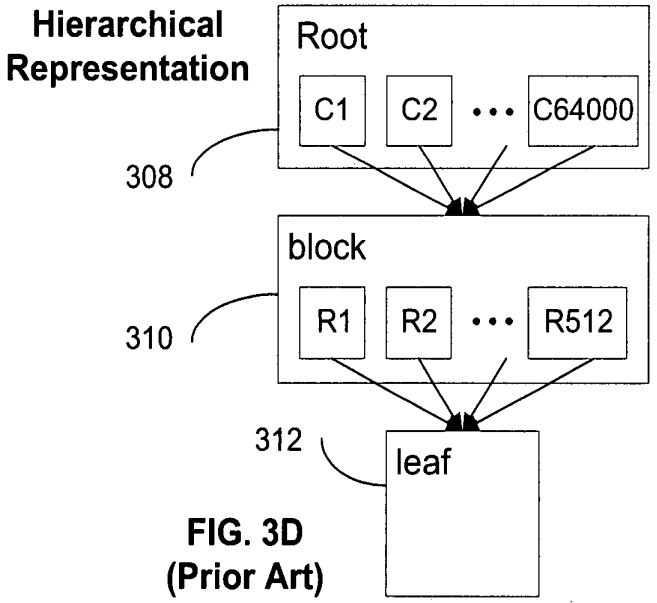


FIG. 3D (Prior Art)

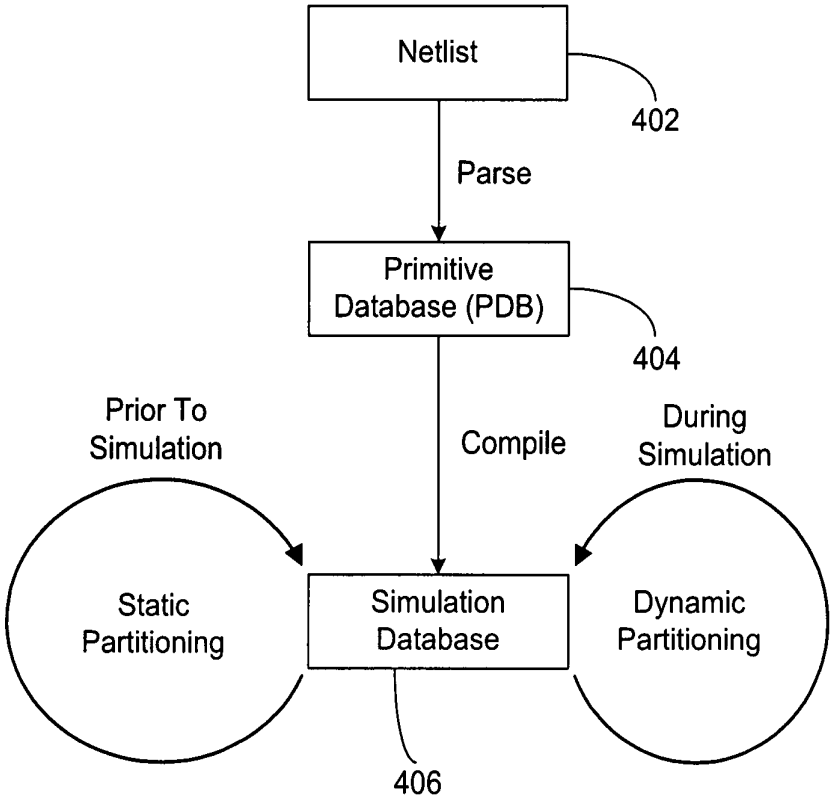


FIG. 4 (Prior Art)

Static Partitioning

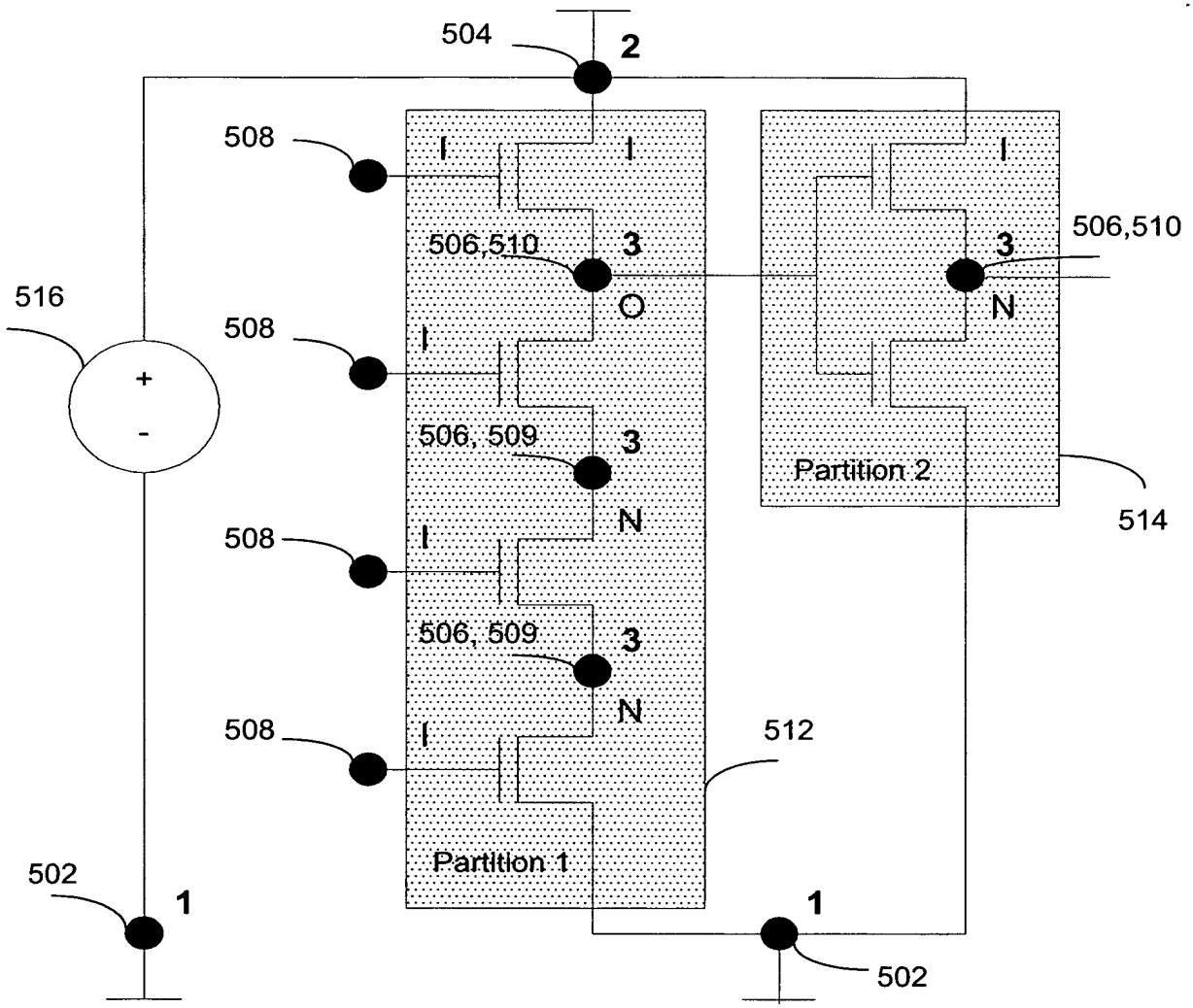


FIG. 5 (Prior Art)

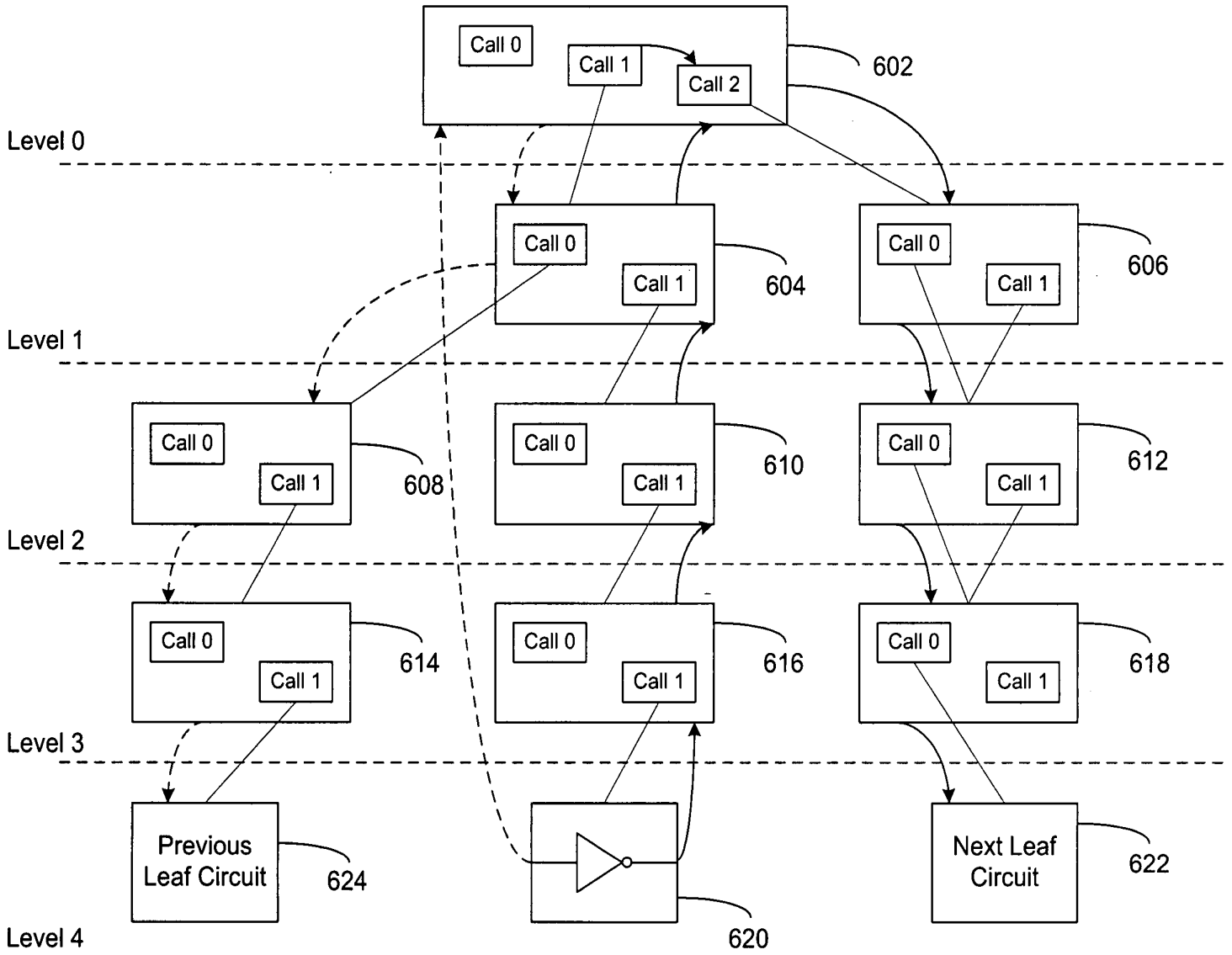


FIG. 6 (Prior Art)

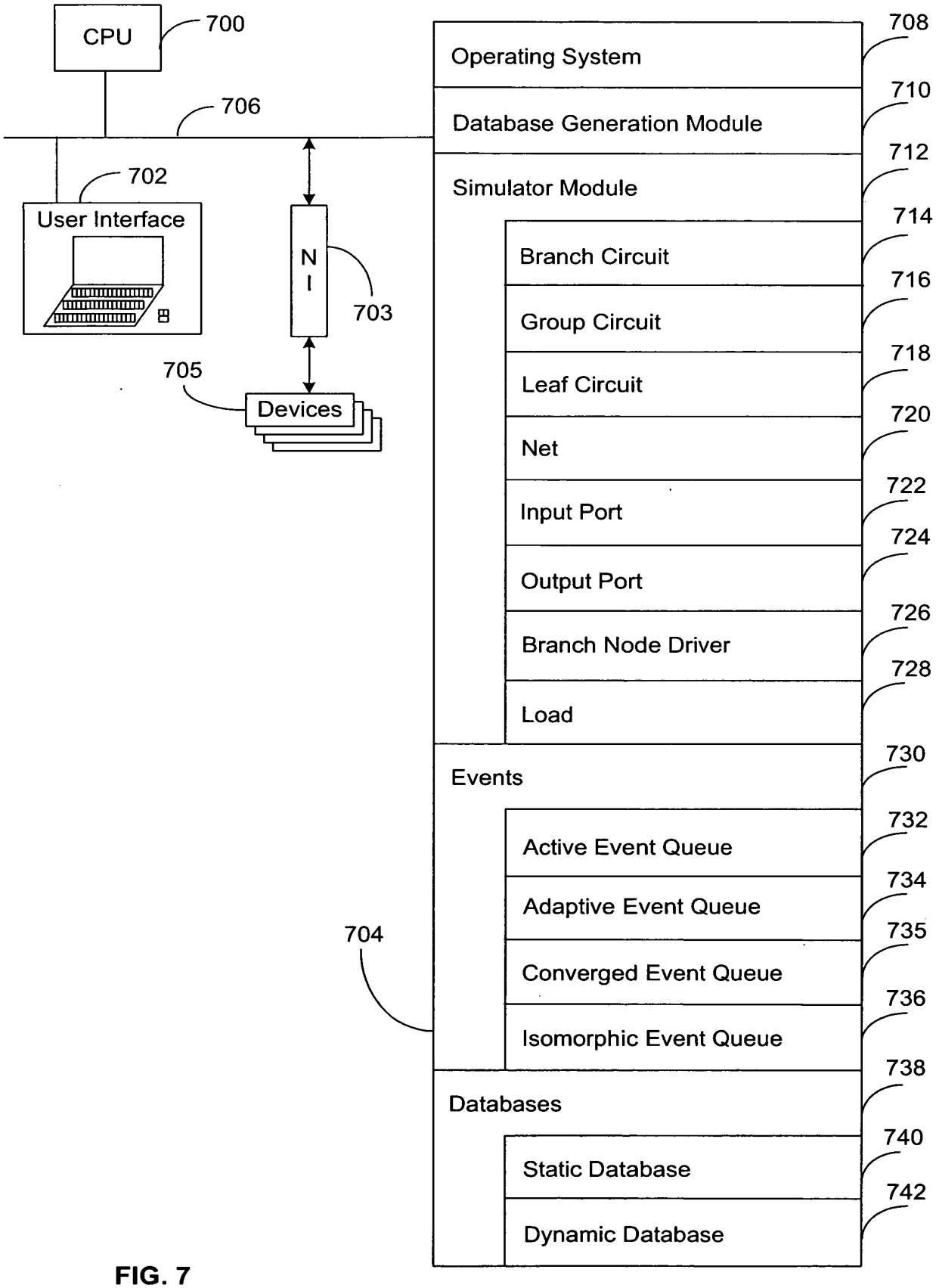

CPU
700
706
User Interface
702
N
I
703
705
Devices
704
Operating System
708
Database Generation Module
710
Simulator Module
712
Branch Circuit
714
Group Circuit
716
Leaf Circuit
718
Net
720
Input Port
722
Output Port
724
Branch Node Driver
726
Load
728
Events
730
Active Event Queue
732
Adaptive Event Queue
734
Converged Event Queue
735
Isomorphic Event Queue
736
Databases
738
Static Database
740
Dynamic Database
742

FIG. 7

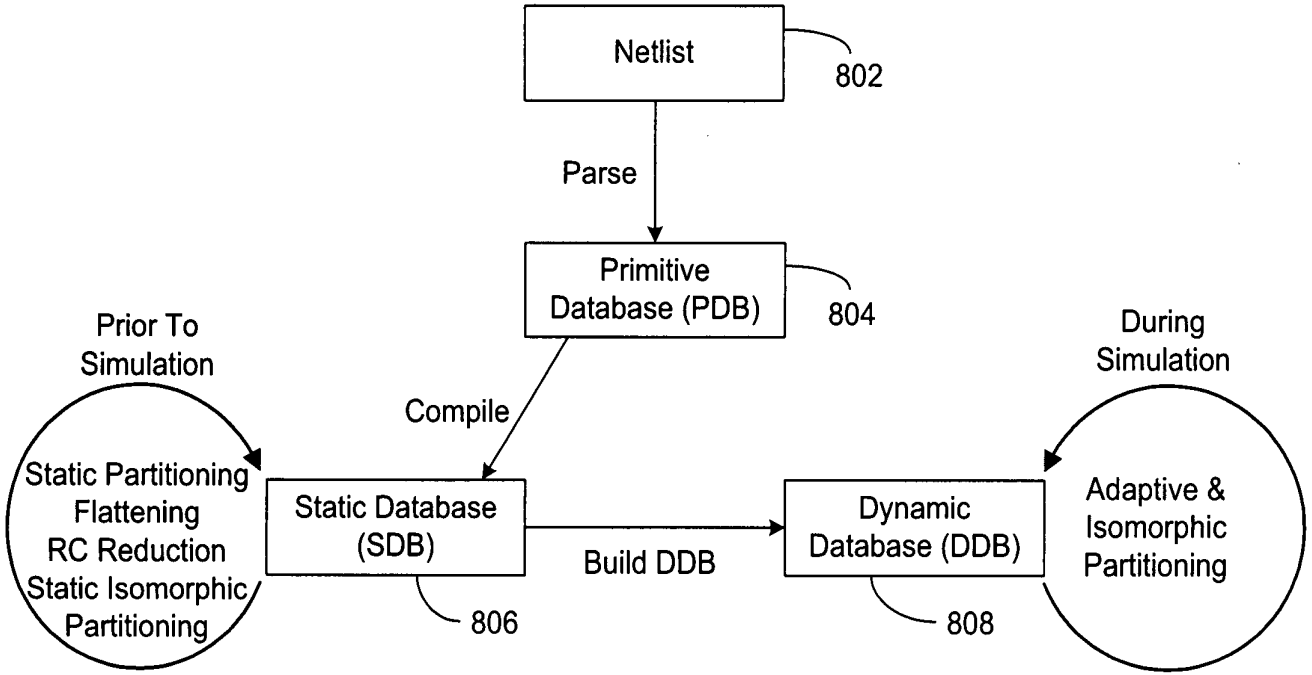

Netlist
802
Parse
Primitive
Database (PDB)
804
Prior To
Simulation
During
Simulation
Compile
Static Partitioning
Flattening
RC Reduction
Static Isomorphic
Partitioning
Static Database
(SDB)
Build DDB
Dynamic
Database (DDB)
Adaptive &
Isomorphic
Partitioning
806
808

FIG. 8A

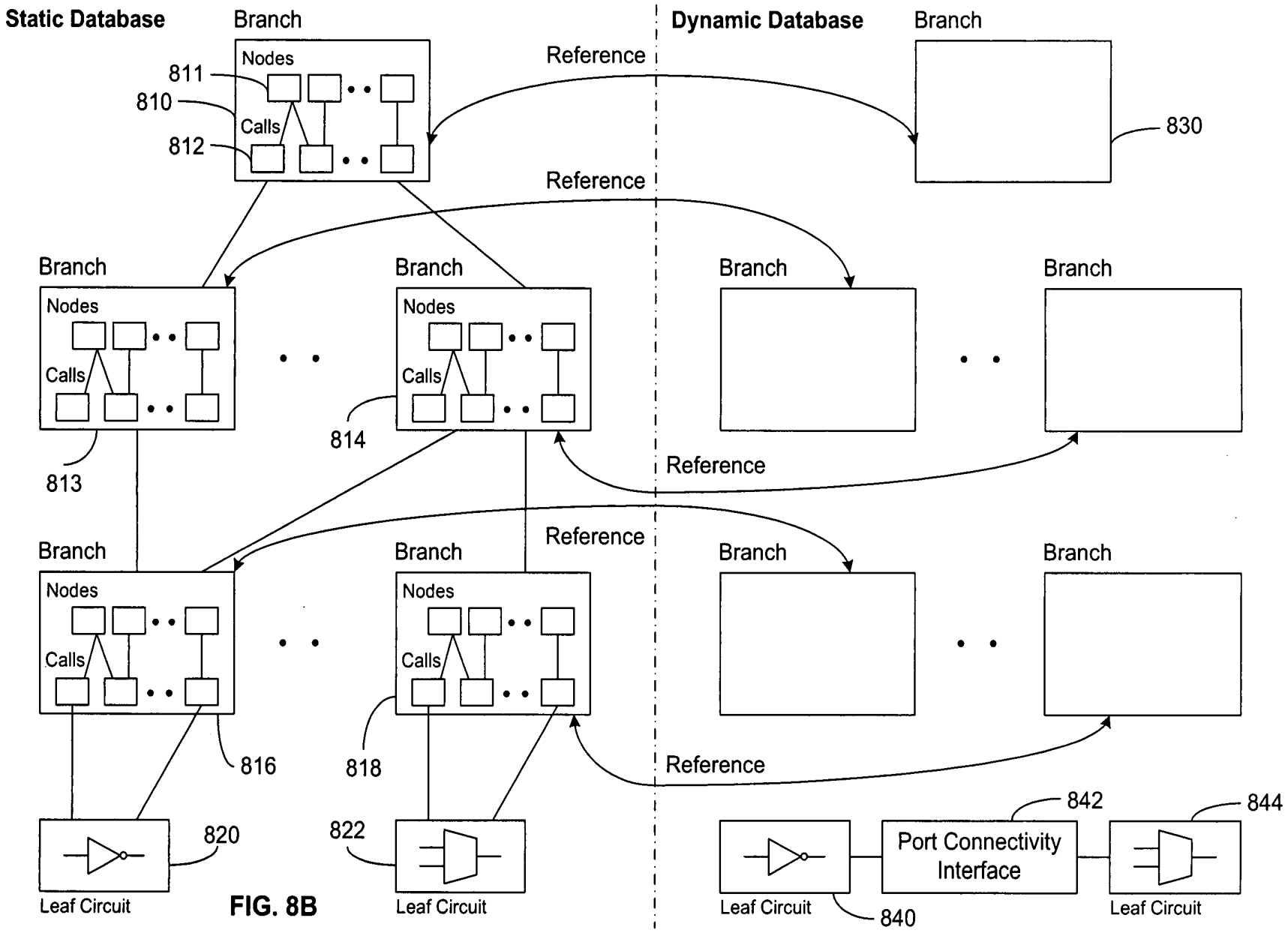

Static Database
Branch
Nodes
Calls
811
810
812
Reference
Dynamic Database
Branch
830
Reference
Branch
Nodes
Calls
813
814
Branch
Nodes
Calls
Branch
Branch
Reference
Branch
Nodes
Calls
816
818
Branch
Nodes
Calls
Branch
Branch
Reference
Reference
820
822
842
844
Port Connectivity Interface
Leaf Circuit
Leaf Circuit
840
Leaf Circuit
Leaf Circuit

FIG. 8B

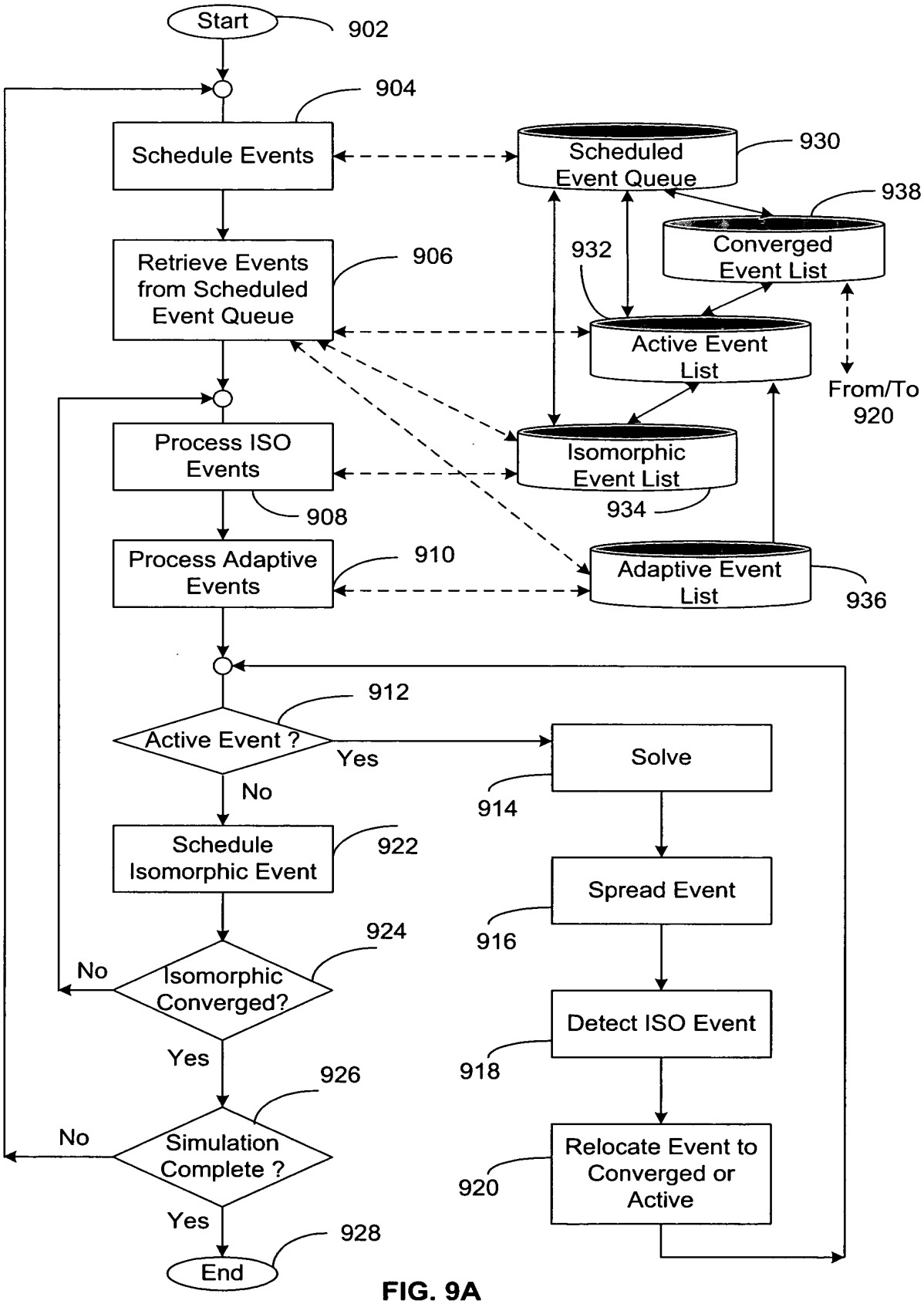

Start
902
904
Schedule Events
Scheduled Event Queue
930
938
Converged Event List
932
Retrieve Events from Scheduled Event Queue
906
Active Event List
From/To 920
Process ISO Events
Isomorphic Event List
934
908
Process Adaptive Events
910
Adaptive Event List
936
912
Active Event ?
Yes
No
Solve
914
Schedule Isomorphic Event
922
Spread Event
916
924
No
Isomorphic Converged?
Detect ISO Event
918
Yes
926
No
Simulation Complete ?
Relocate Event to Converged or Active
920
Yes
928
End

FIG. 9A

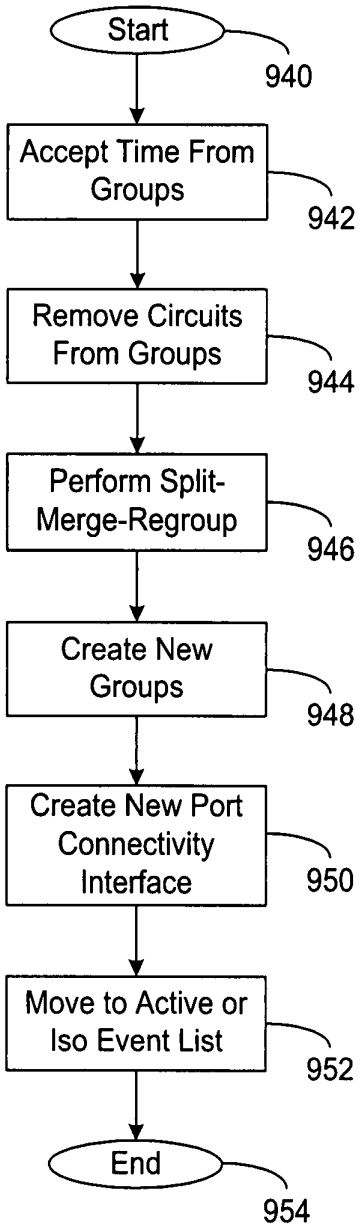

Start
940
Accept Time From Groups
942
Remove Circuits From Groups
944
Perform Split-Merge-Regroup
946
Create New Groups
948
Create New Port Connectivity Interface
950
Move to Active or Iso Event List
952
End
954

FIG. 9B

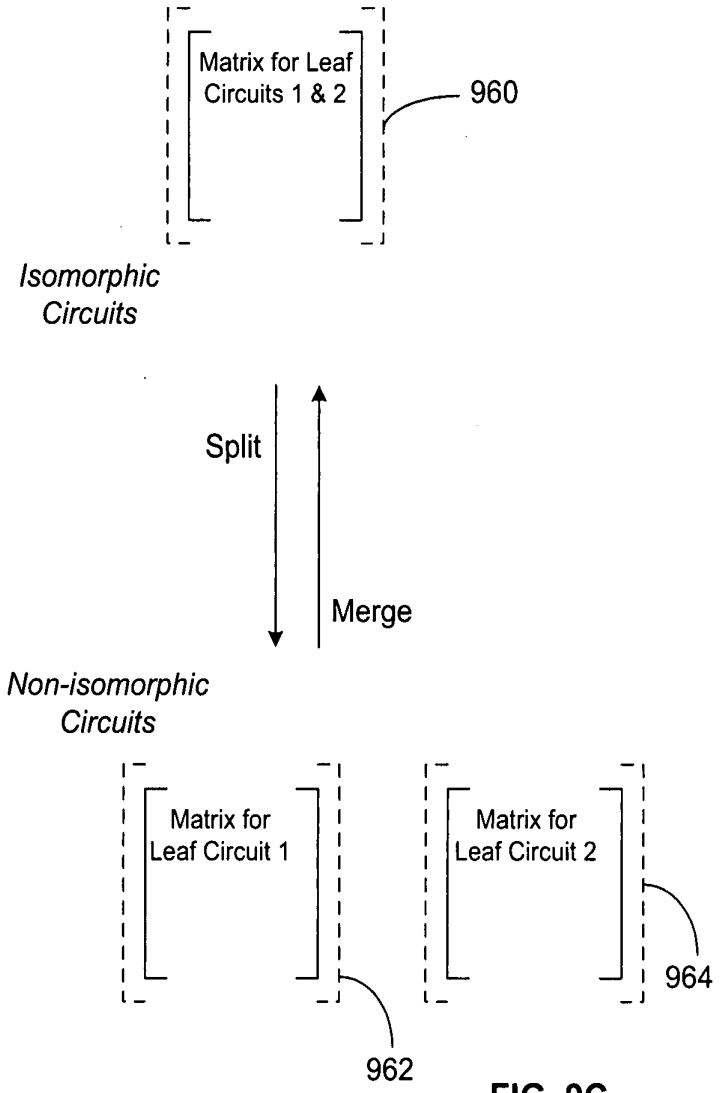

Matrix for Leaf Circuits 1 & 2
960
Isomorphic Circuits
Split
Merge
Non-isomorphic Circuits
Matrix for Leaf Circuit 1
Matrix for Leaf Circuit 2
964
962

FIG. 9C

FIG. 10A

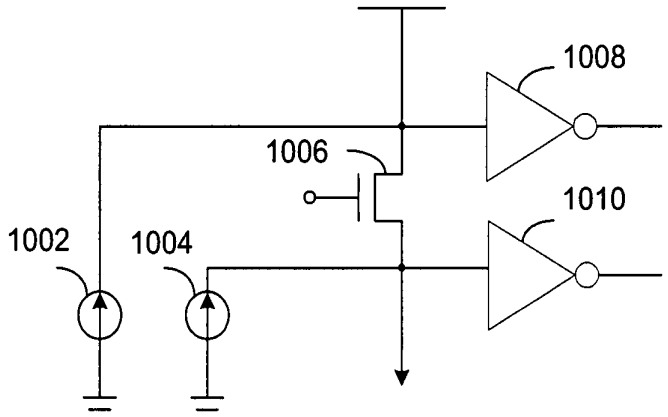
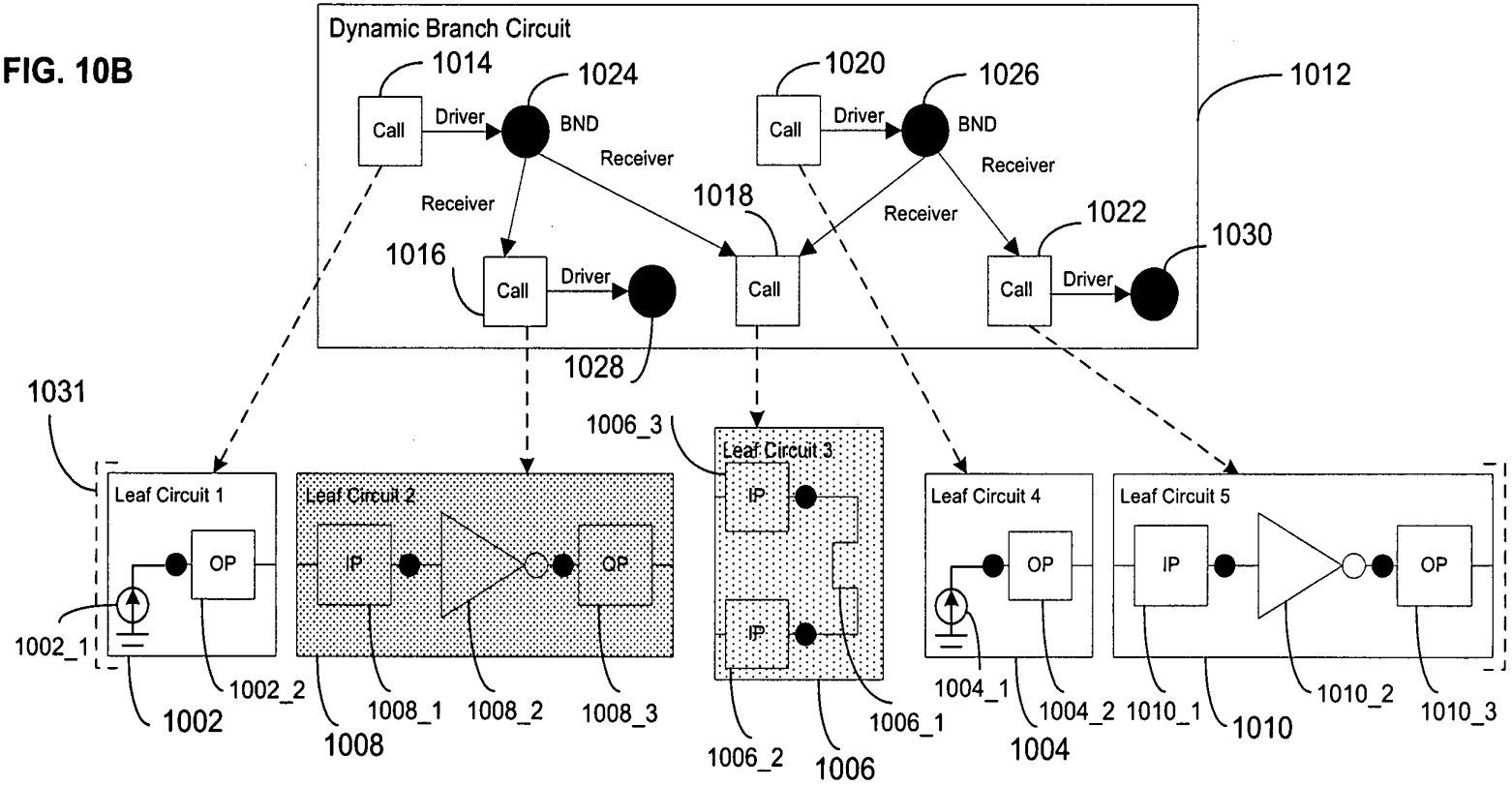


FIG. 10B



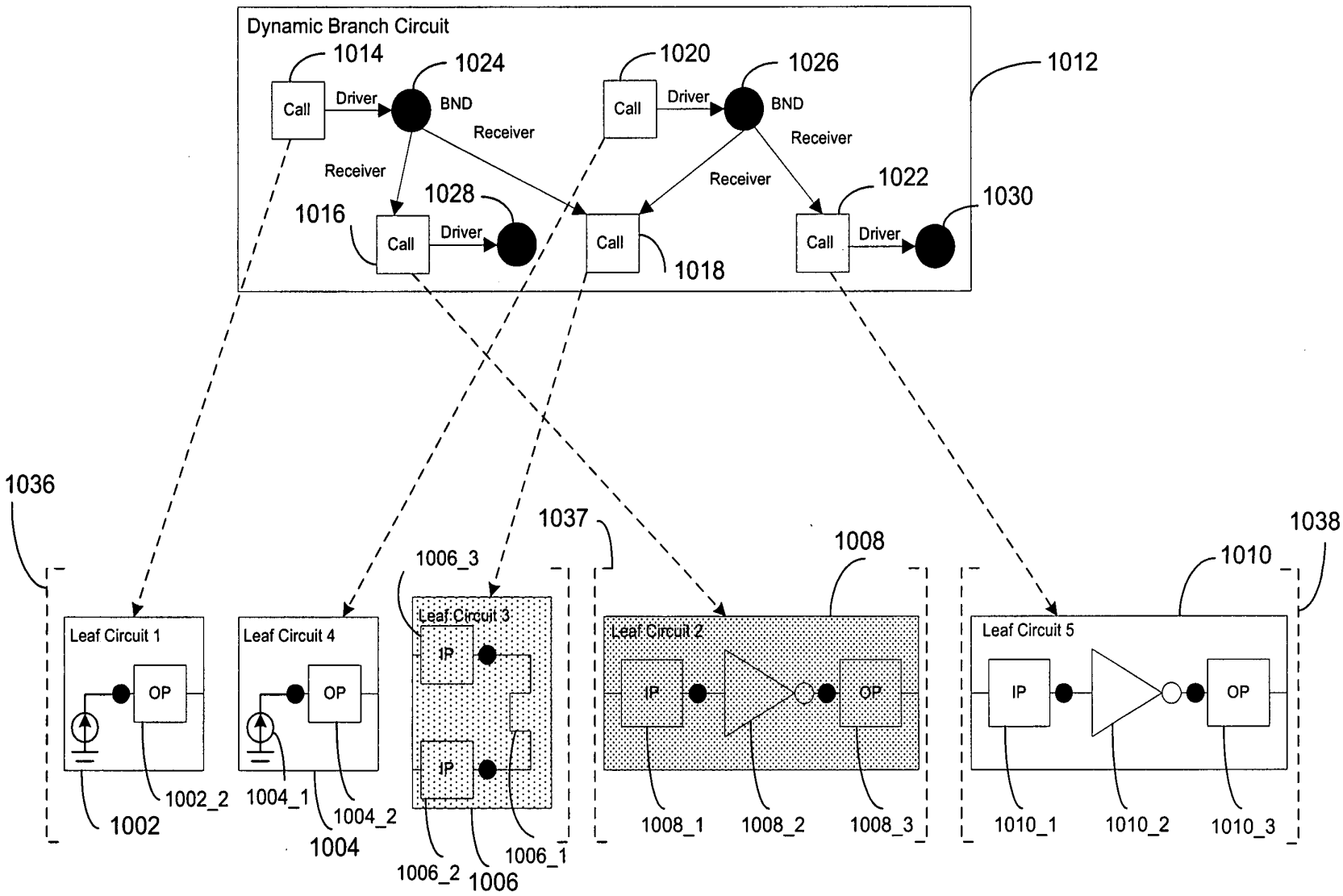

Dynamic Branch Circuit
1012
1014
1024
1020
1026
Call
Driver
BND
Receiver
Call
Driver
BND
Receiver
Receiver
Receiver
1028
1016
1022
1030
Call
Driver
Call
1018
Call
Driver
1036
1037
1038
1008
1010
1006_3
Leaf Circuit 1
Leaf Circuit 4
Leaf Circuit 3
Leaf Circuit 2
Leaf Circuit 5
IP
OP
1002_2
1002
1004_1
1004_2
1004
1006_2
1006
1006_1
1008_1
1008_2
1008_3
1010_1
1010_2
1010_3

FIG. 10C

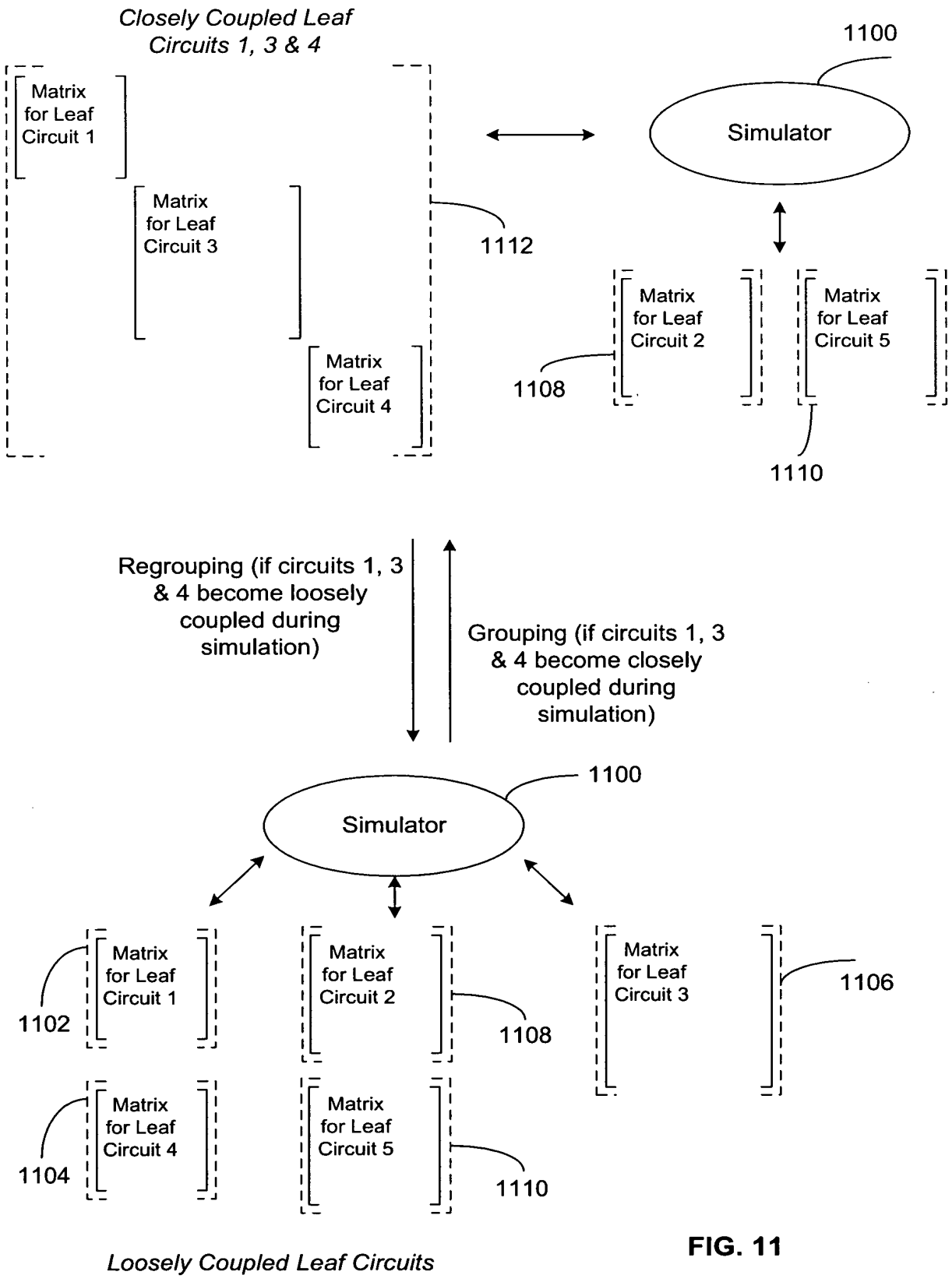

Closely Coupled Leaf Circuits 1, 3 & 4
Matrix for Leaf Circuit 1
Matrix for Leaf Circuit 3
Matrix for Leaf Circuit 4
1112
1100
Simulator
Matrix for Leaf Circuit 2
1108
Matrix for Leaf Circuit 5
1110
Regrouping (if circuits 1, 3 & 4 become loosely coupled during simulation)
Grouping (if circuits 1, 3 & 4 become closely coupled during simulation)
1100
Simulator
Matrix for Leaf Circuit 1
1102
Matrix for Leaf Circuit 2
1108
Matrix for Leaf Circuit 3
1106
Matrix for Leaf Circuit 4
1104
Matrix for Leaf Circuit 5
1110
Loosely Coupled Leaf Circuits

FIG. 11

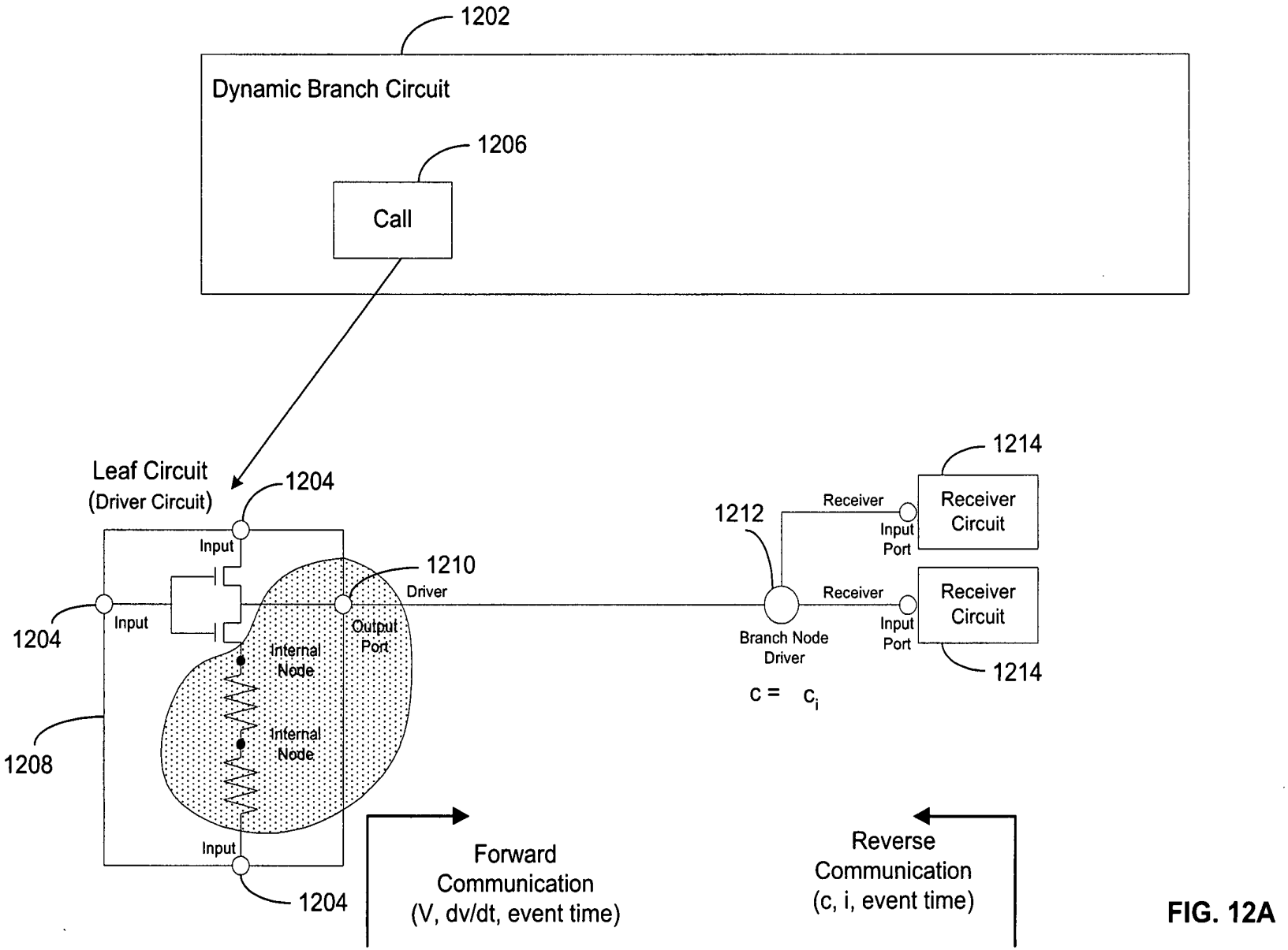

1202
Dynamic Branch Circuit
1206
Call
Leaf Circuit
(Driver Circuit)
1204
Input
1210
Driver
1204
Input
Output
Port
Internal
Node
Internal
Node
1208
Input
1204
1212
Receiver
Input
Port
Receiver
Circuit
1214
Receiver
Input
Port
Receiver
Circuit
1214
Branch Node
Driver
c = c_i
Forward
Communication
(V, dv/dt, event time)
Reverse
Communication
(c, i, event time)

FIG. 12A

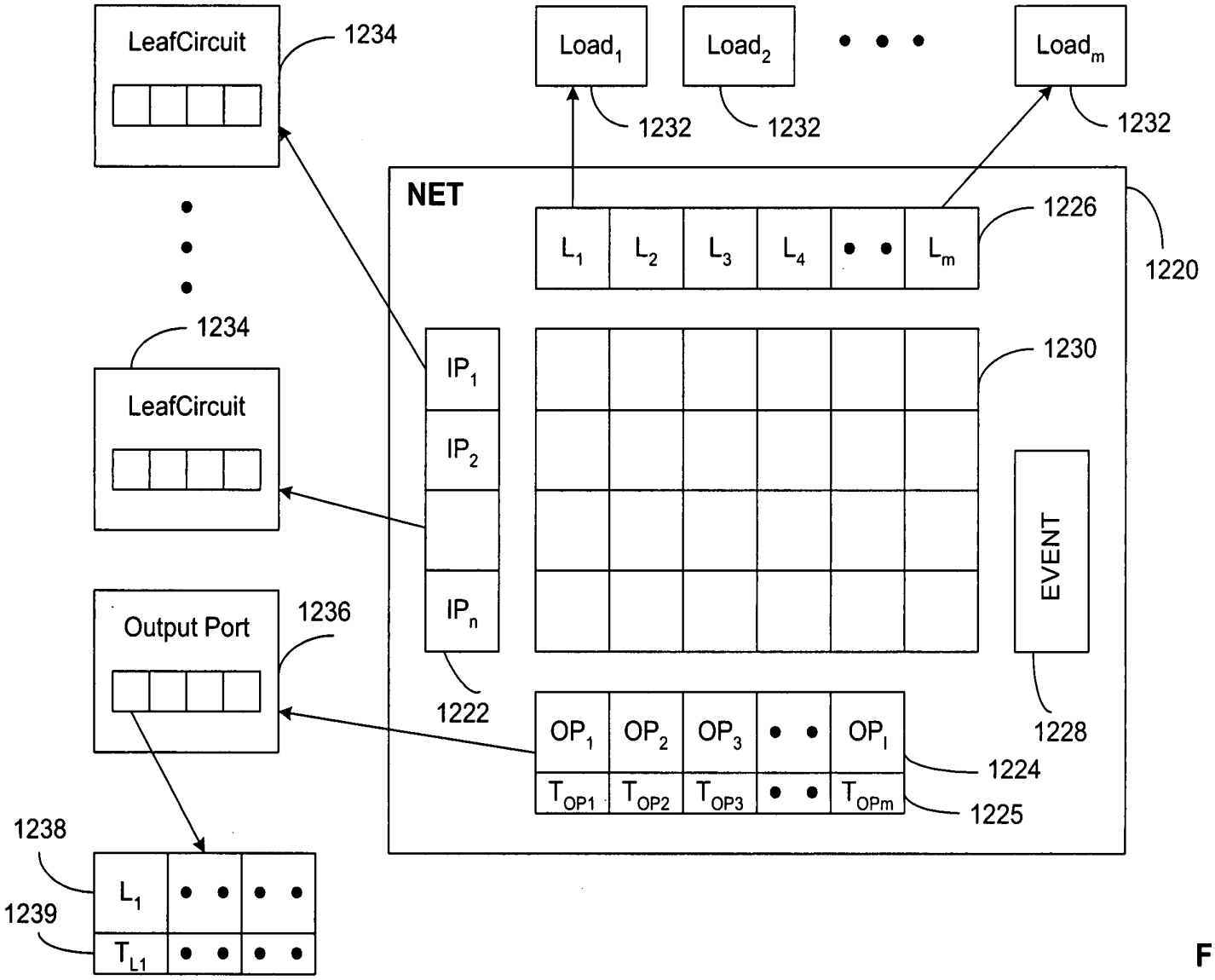

LeafCircuit
1234
Load1
Load2
Loadm
1232
1232
1232
NET
L1
L2
L3
L4
Lm
1226
1220
1234
LeafCircuit
IP1
IP2
IPn
1230
EVENT
1222
1228
Output Port
1236
OP1
OP2
OP3
OPl
1224
TOP1
TOP2
TOP3
TOPm
1225
1238
L1
1239
TL1

FIG. 12B

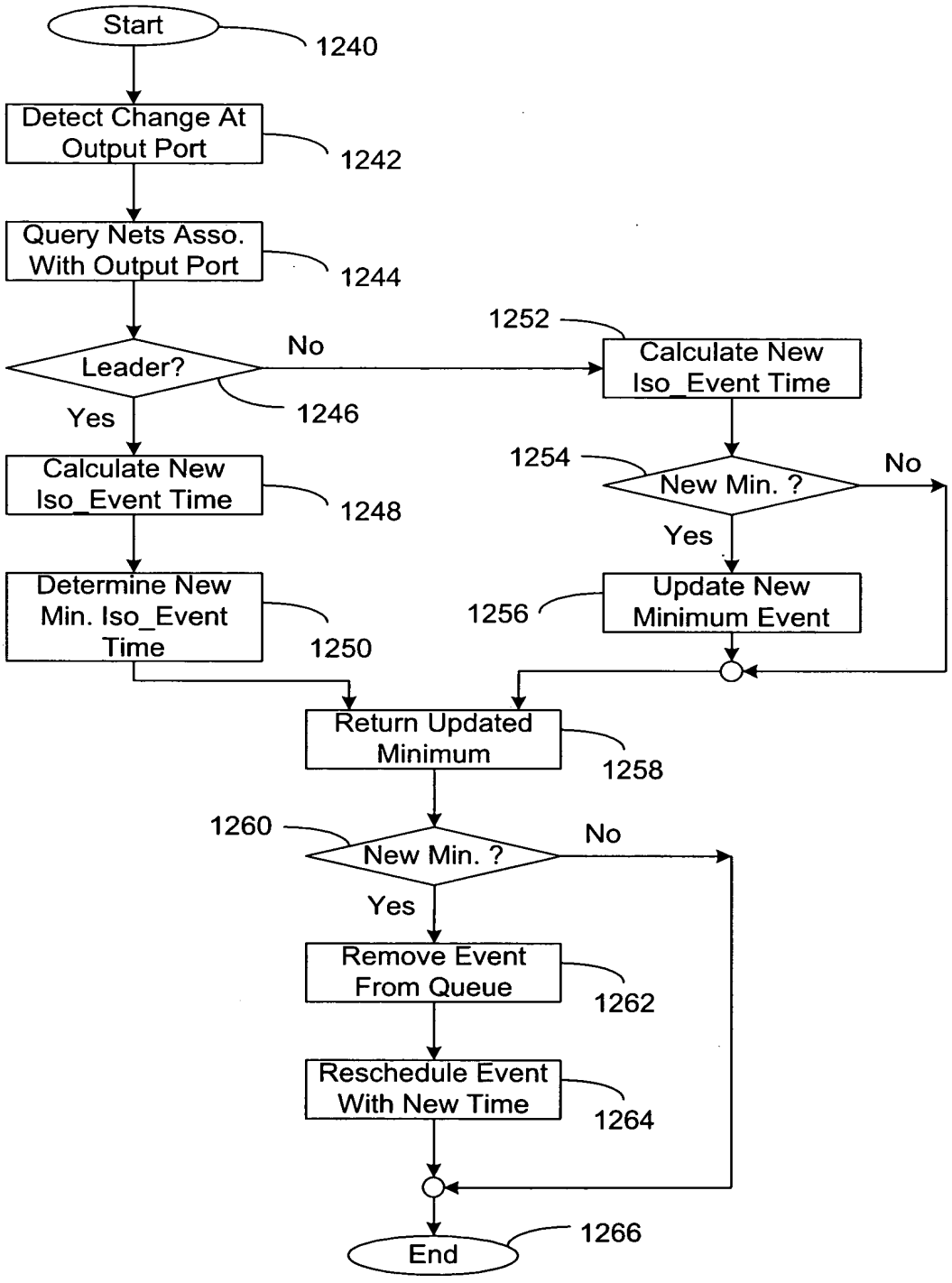

Start
1240
Detect Change At Output Port
1242
Query Nets Asso. With Output Port
1244
Leader?
No
1246
Yes
Calculate New Iso_Event Time
1248
Determine New Min. Iso_Event Time
1250
1252
Calculate New Iso_Event Time
1254
New Min. ?
No
Yes
1256
Update New Minimum Event
Return Updated Minimum
1258
1260
New Min. ?
No
Yes
Remove Event From Queue
1262
Reschedule Event With New Time
1264
End
1266

FIG. 12C

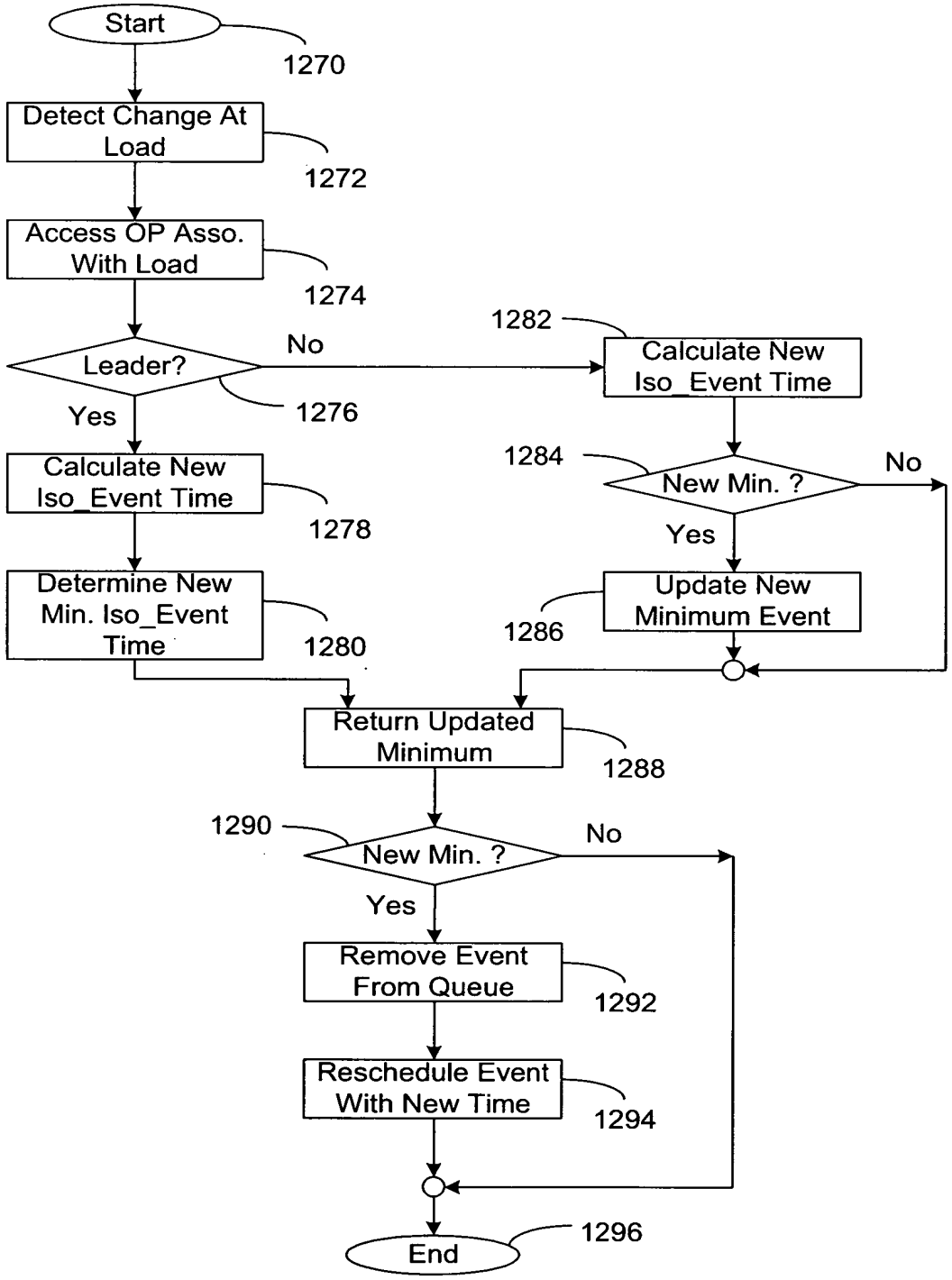

Start
1270
Detect Change At Load
1272
Access OP Asso. With Load
1274
Leader?
1276
No
Yes
1282
Calculate New Iso_Event Time
1284
New Min. ?
No
Yes
Update New Minimum Event
1286
Calculate New Iso_Event Time
1278
Determine New Min. Iso_Event Time
1280
Return Updated Minimum
1288
1290
New Min. ?
No
Yes
Remove Event From Queue
1292
Reschedule Event With New Time
1294
End
1296

FIG. 12D

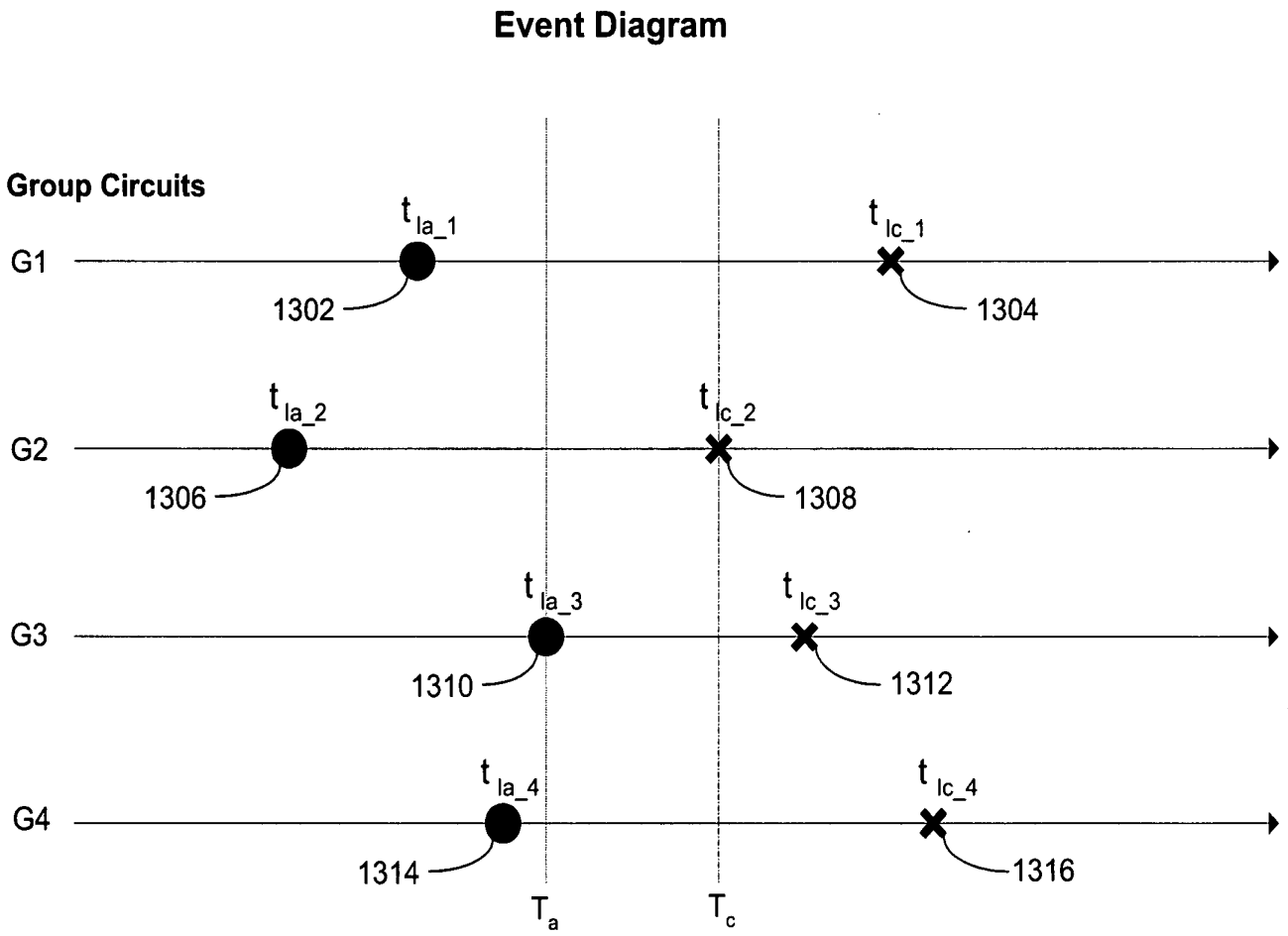

Event Diagram
Group Circuits
G1
G2
G3
G4
t_{Ia_1}
t_{Ic_1}
1302
1304
t_{Ia_2}
t_{Ic_2}
1306
1308
t_{Ia_3}
t_{Ic_3}
1310
1312
t_{Ia_4}
t_{Ic_4}
1314
1316
T_a
T_c

FIG. 13A

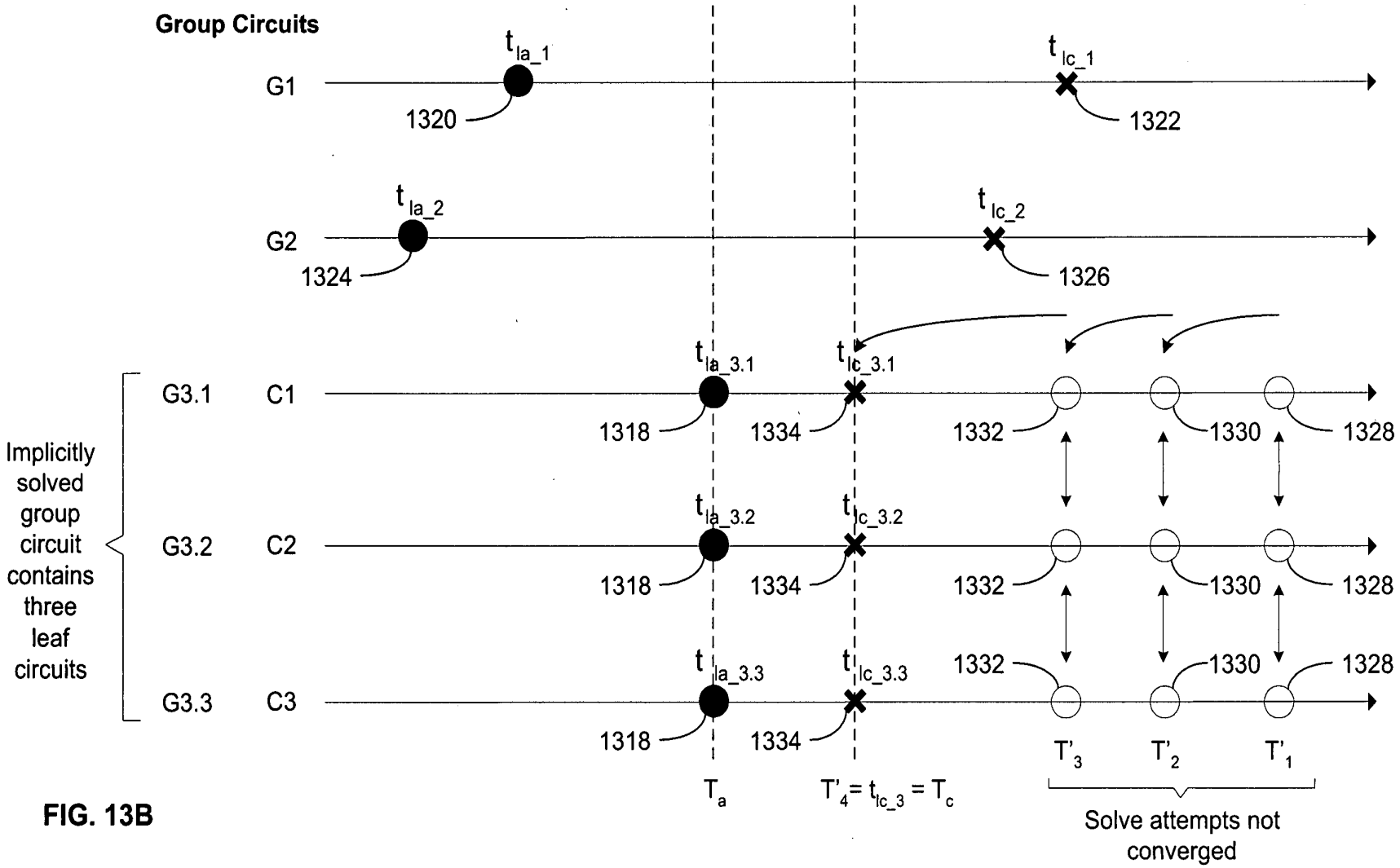

Group Circuits
G1
t_{Ia_1}
1320
t_{Ic_1}
1322
G2
t_{Ia_2}
1324
t_{Ic_2}
1326
G3.1
C1
$t_{Ia\_3.1}$
$t_{Ic\_3.1}$
1318
1334
1332
1330
1328
G3.2
C2
$t_{Ia\_3.2}$
$t_{Ic\_3.2}$
1318
1334
1332
1330
1328
G3.3
C3
$t_{Ia\_3.3}$
$t_{Ic\_3.3}$
1318
1334
1332
1330
1328
Implicitly solved group circuit contains three leaf circuits
T'_3
T'_2
T'_1
T_a
$T'_4 = t_{Ic\_3} = T_c$
Solve attempts not converged

FIG. 13B

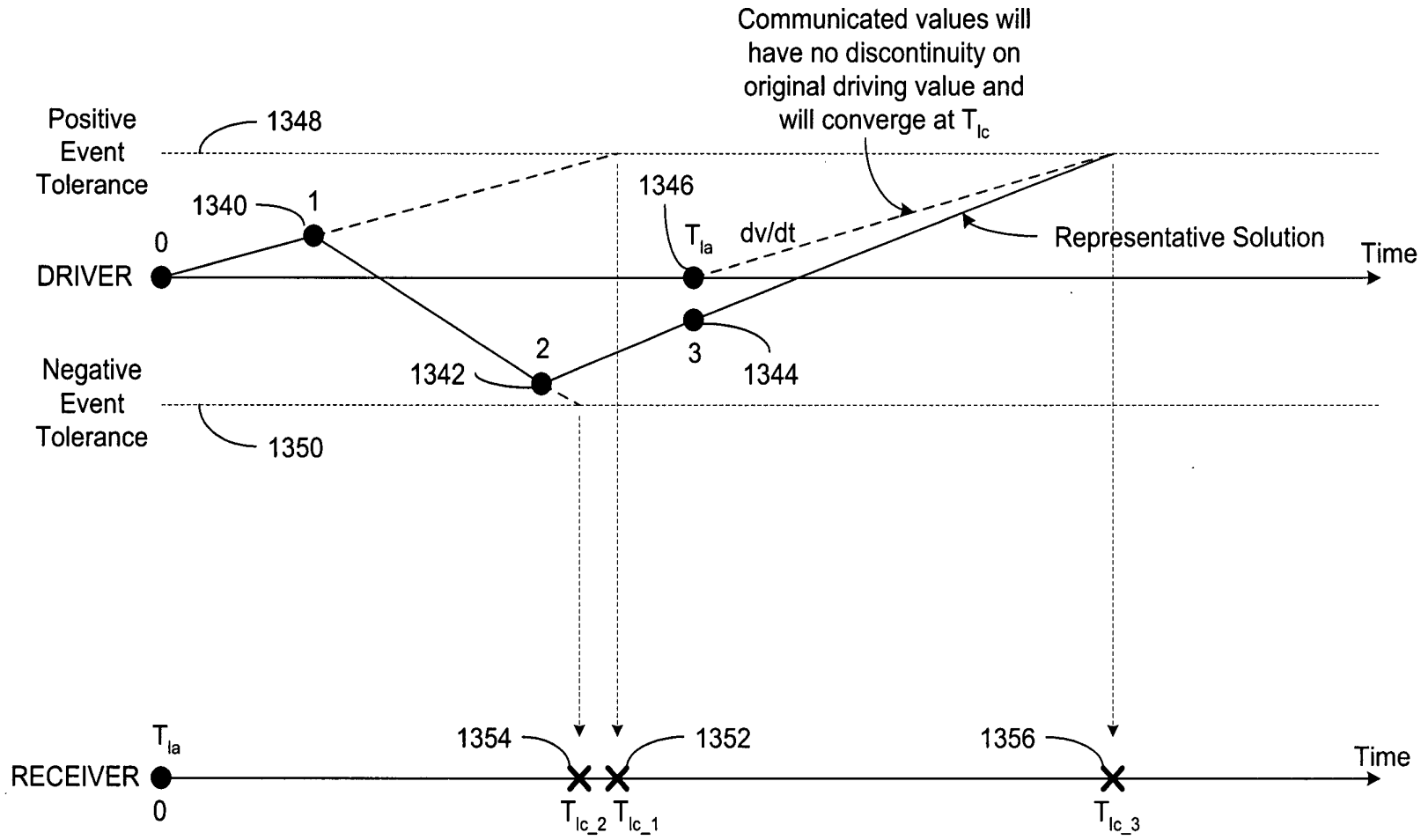

Communicated values will have no discontinuity on original driving value and will converge at T_{lc}
Positive Event Tolerance
1348
1340
1
0
DRIVER
1346
T_{la}
dv/dt
Representative Solution
Time
2
1342
3
1344
Negative Event Tolerance
1350
T_{la}
RECEIVER
0
1354
1352
1356
T_{lc_2}
T_{lc_1}
T_{lc_3}
Time

FIG. 13C

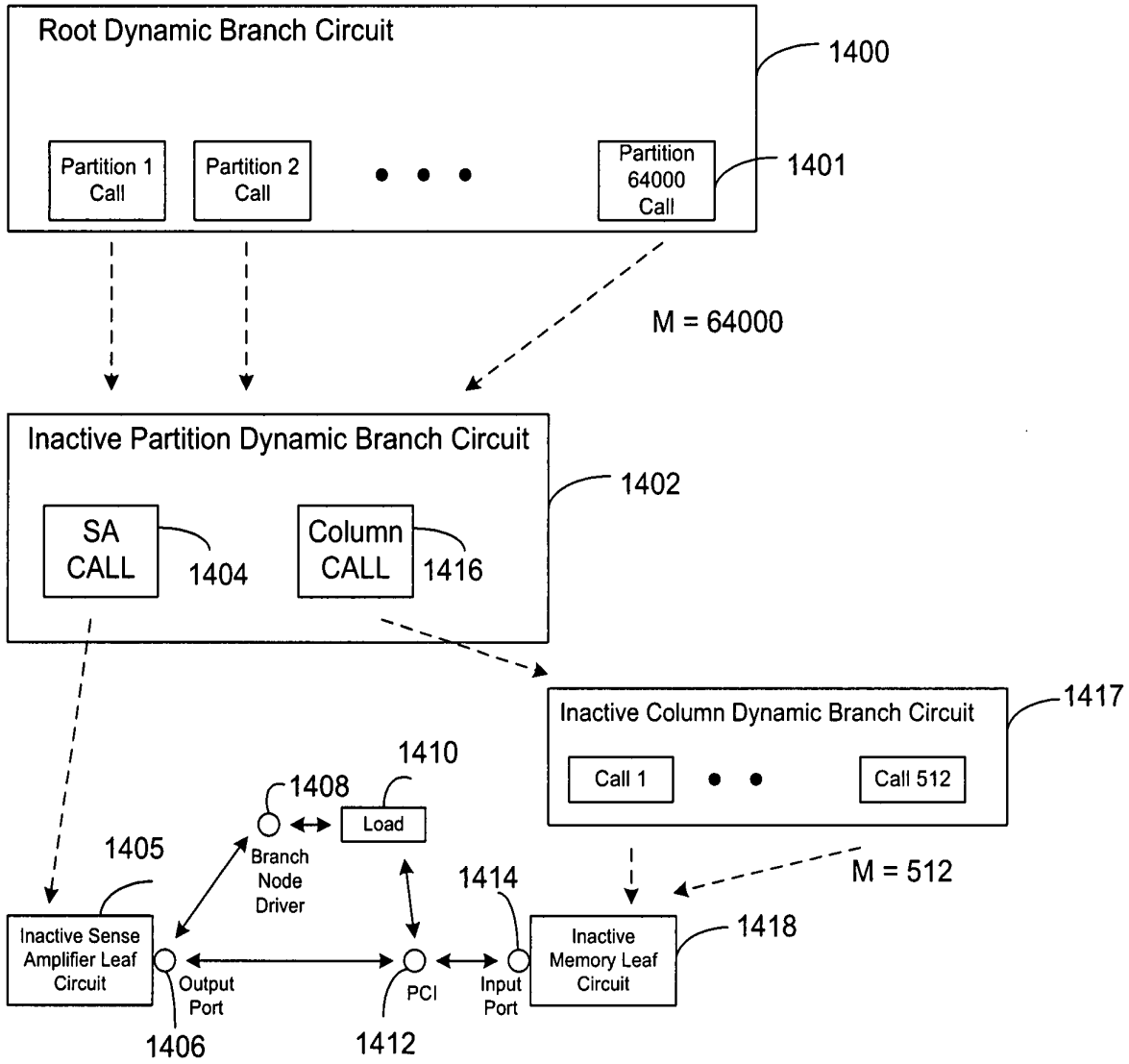


FIG. 14A

Initial State

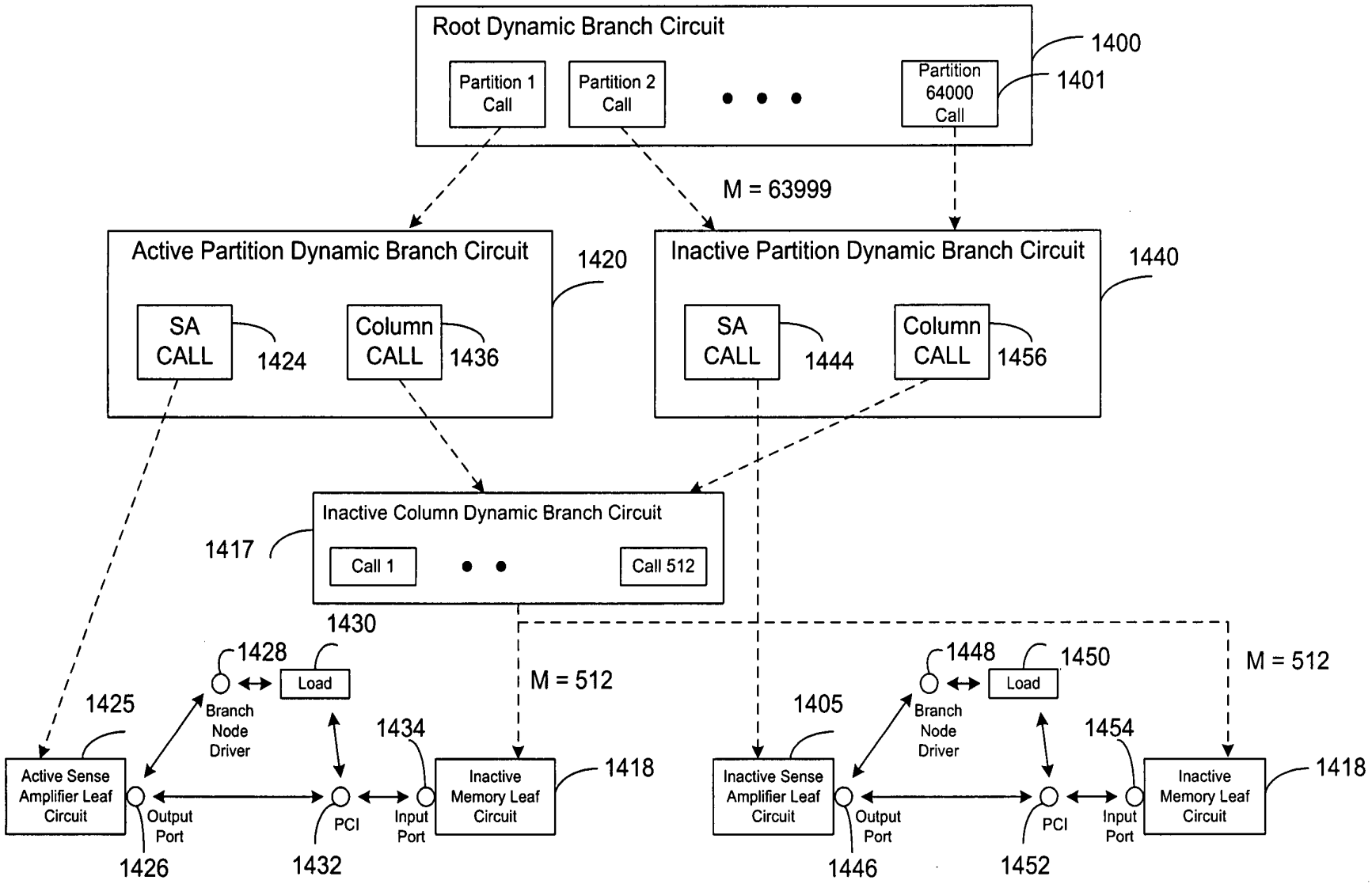


FIG. 14B

During Simulation When One Of The Sense Amplifiers Is Active And The Column Driven By The Sense Amplifier Is Inactive

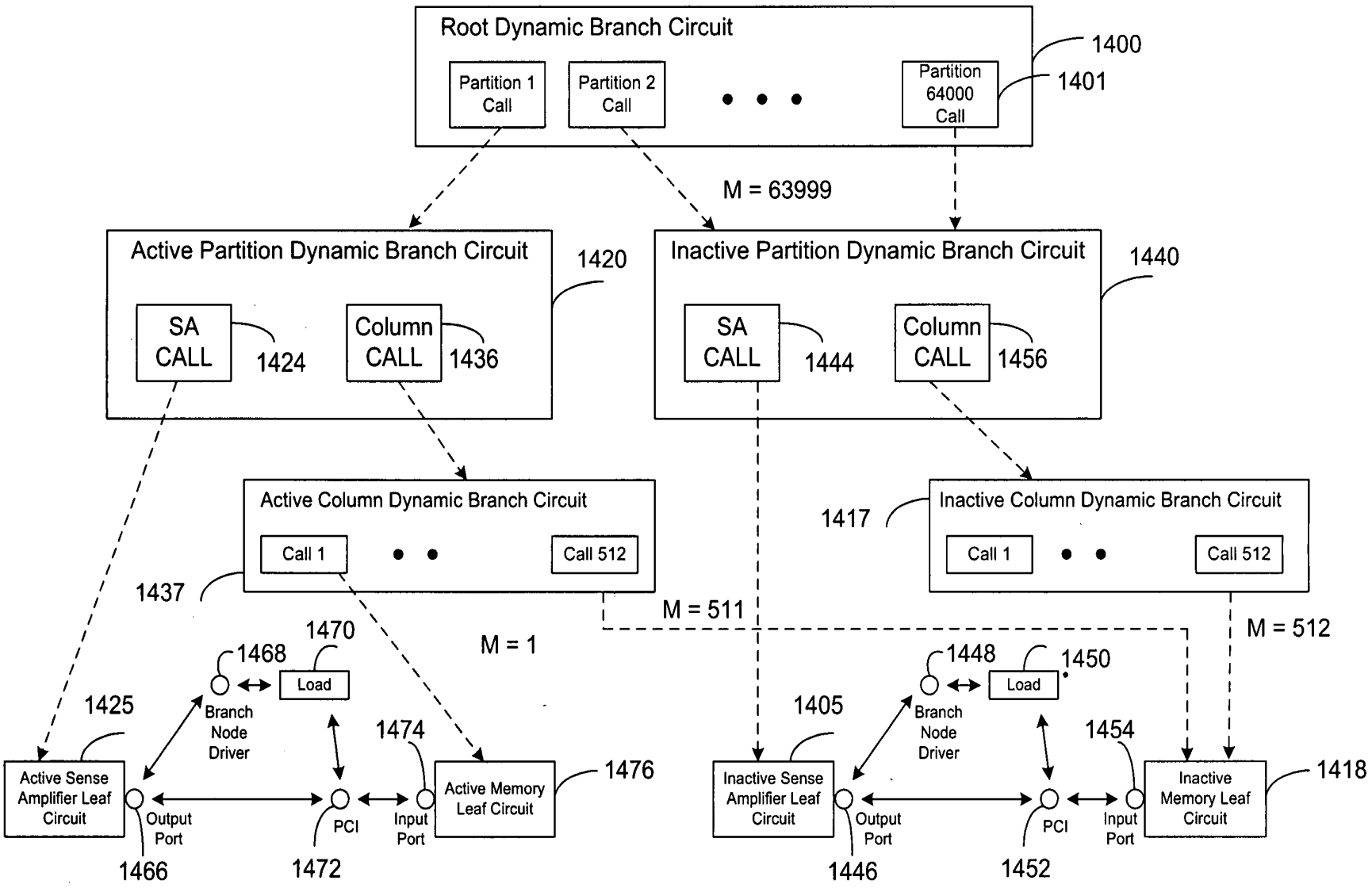


FIG. 14C During Simulation When One Of The Memory Leaf Circuits Driven By The Corresponding Active Sense Amplifier Is Active